Investigation of a USRP FPGA Platform for Quantum Sensing and Control

Aaron Wubshet

Agenda

Background

Algorithm development

Hardware Realization

Conclusion

Next Steps

Questions

Logistics & Scope

FEASIBILITY STUDY FOLLOW UP TO LDRD

POSTER SESSION, SEMINAR, AND MASTER'S THESIS

USRP PLATFORM FOR SUPERCONDUCTING QUANTUM SENSING

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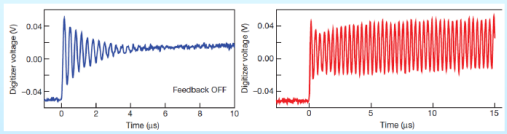
BACKGROUND & APPLICATIONS

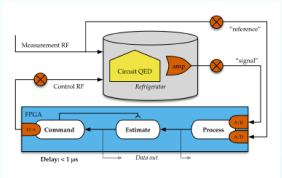
- DOE National Strategic Computing Initiative and LLNL's HPC, Simulation, and Data Science core competency
- We want to rapidly control a superconducting qubit
  - Desirable output

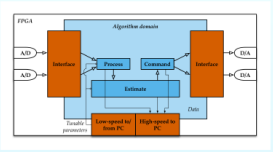


Figures from Vijay, R. et al Stabilizing Rabi Oscillations in a Superconducting Qubit Using Quantum Feedback, Nature 2012

- Axion detection research
- Quantum information processing

EXPERIMENTAL SETUP





Kintex-7

Virtex-6

- Implement complete algorithm on USRP with timing constraints met
- Finalize thesis project experiment

June — Sept. — Dec

- Migrate "process" onto USRP
- Begin investigating universal portability of HDL generated

- Gather materials & relevant toolchains required
- Complete data collection, analysis, & thesis

Progress

- Synthesis:
  - Resource utilization determined
  - Netlist generated
- Design:
  - Leverage and adapt existing IP
  - Simulate and validate functional behavior via testbench
- Place & Route:
  - Timing constraints
  - Programming file generated

- Combining multiple toolchains into cohesive workflow
- Created VHDL "wrapper" to enable portability of HDL being generated
- Validation of USRP implementation
  - Unique testbench for USRP platform
  - Additional handshaking required

NEXT STEPS

CURRENT PROJECT

- The goal is to develop and experimentally validate algorithmic, FPGA-based control of a transmon
- Current progress is concentrated on II FPGA, but migration to USRP (and other platforms) is underway
- Modify implementation in order to meet timing requirements

POSSIBLE THESIS EXPERIMENTS

- Implement less computationally intensive control scheme on FPGA (PID, state space, etc)
- Implement processing, control, and estimation in native VHDL to ensure portability
- Validate and characterize SDR capabilities relative to existing testing RF equipment

Acknowledgements & References

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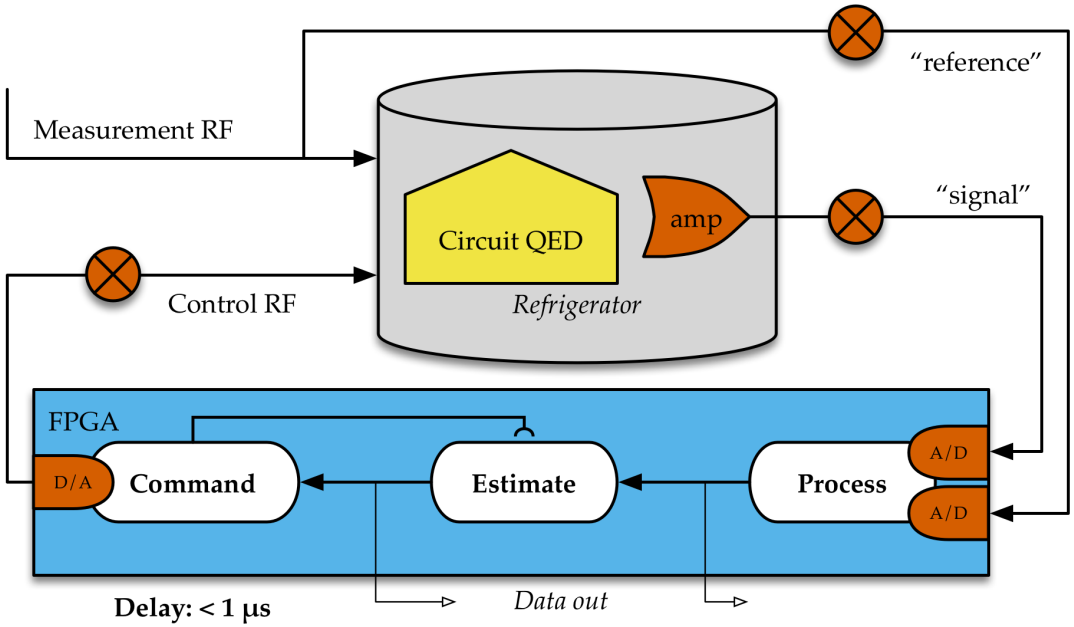
- Vijay, R., et al. "Stabilizing Rabi Oscillations in a Superconducting Qubit Using Quantum Feedback." *Nature News*, Nature Publishing Group, 3 Oct. 2012, www.nature.com/articles/nature11505.
- *Quantum Science Program*, qis.fnal.gov/axion-dark-matter-detection/.

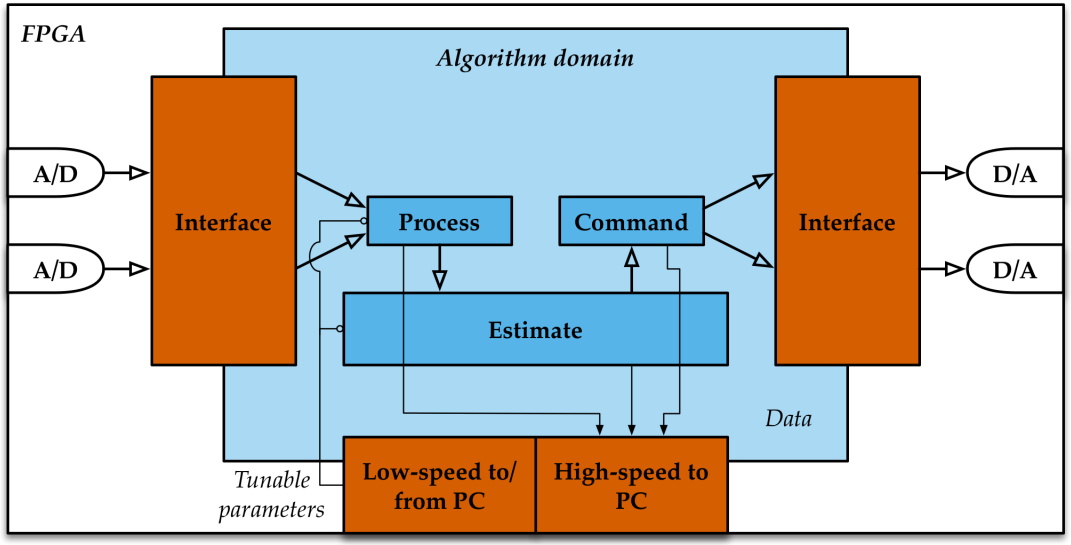
Experimental Apparatus

- 4mK refrigerator
- Circuit QED = superconducting charge qubits as transmons
- External heterodyne



FPGA Interface

- Defining interface for USRP
- Interacting with LabVIEW host
- Configuring RF peripherals



Development Workflow

Simulation

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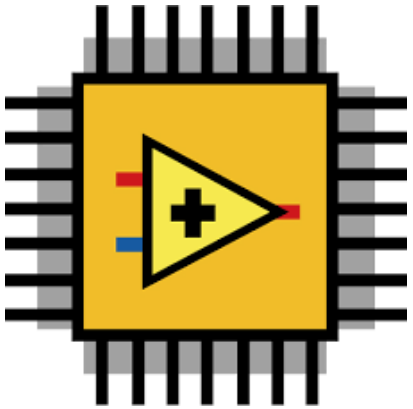
Benchtop Testing

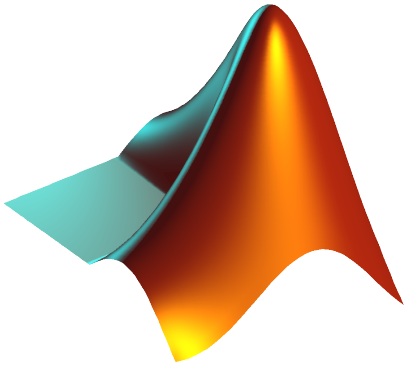
↓

Laboratory Testing

↓

Data Analysis





XILINX®

Quantum Sensing and Control Algorithm (QSCA)

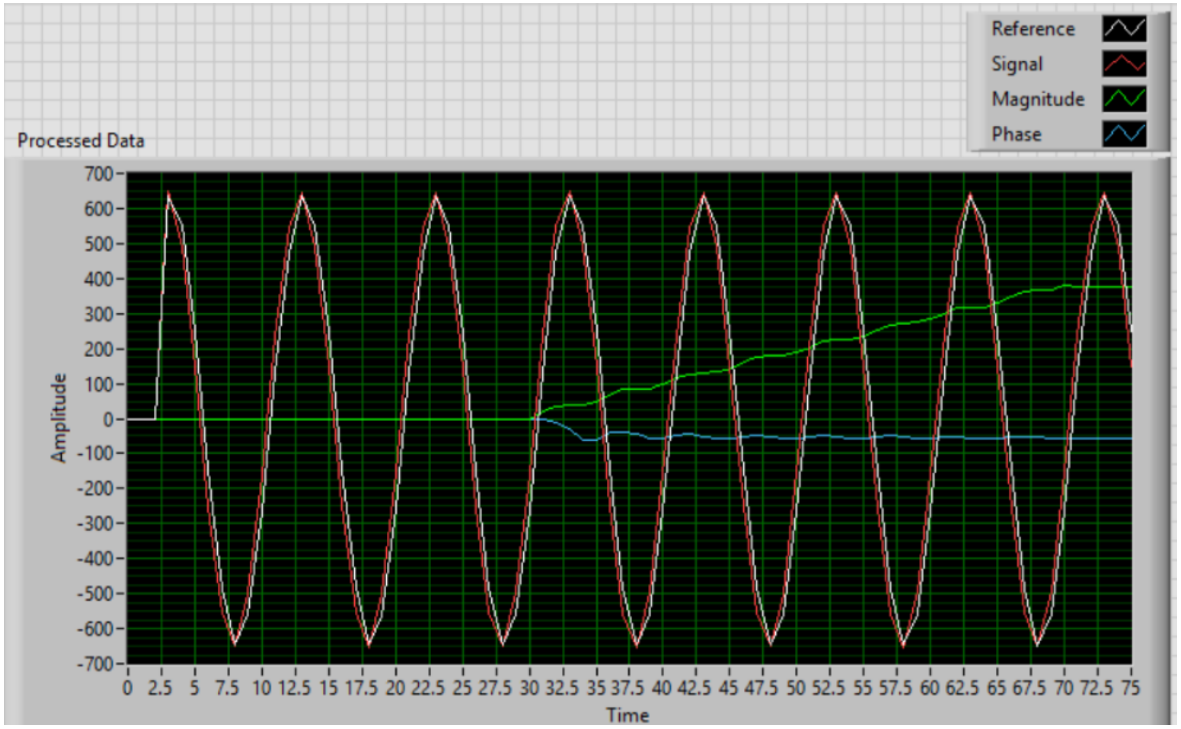
Process

Estimate

Command

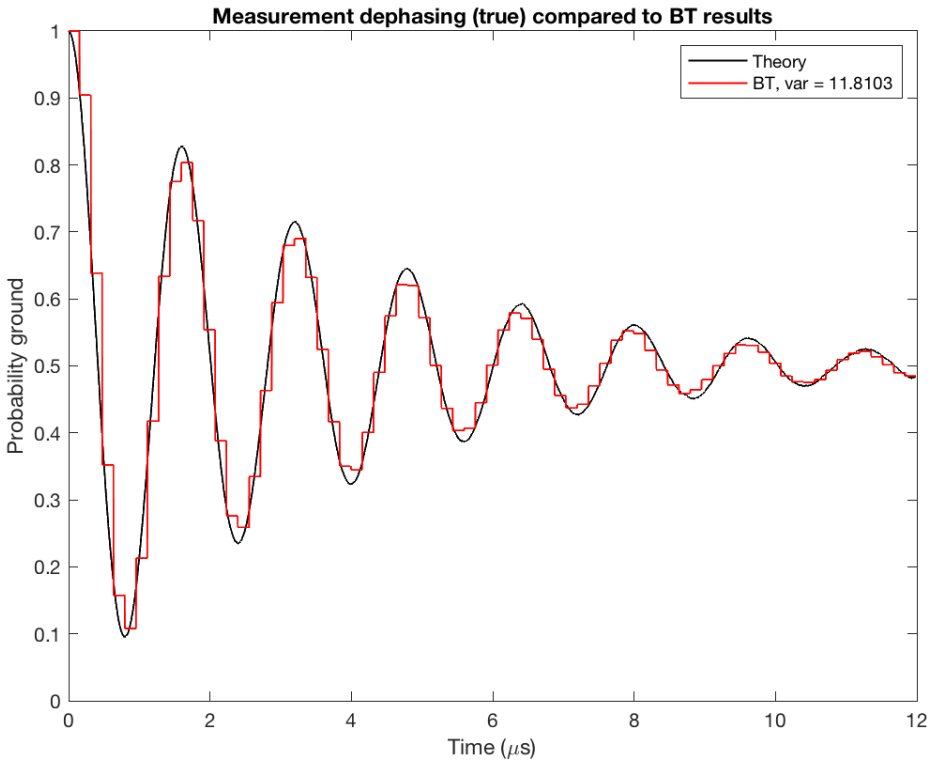
Process

- Moving periodogram algorithm
- CORDIC block to provide phase and magnitude
- Phase difference detection



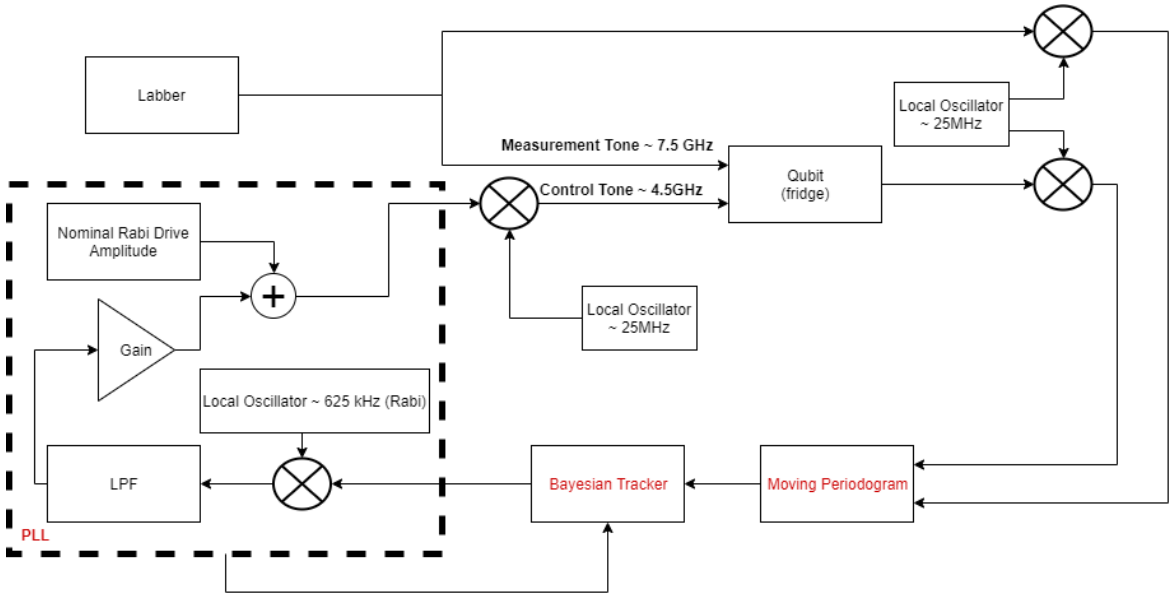
Estimate

- State space model based approach
- Statistical Bayesian update
- Minimum update time 160ns

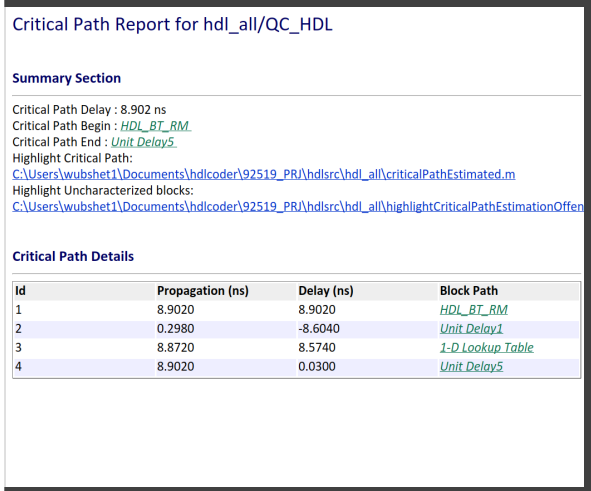


Command

- Lock onto Bayesian Tracker estimate trajectory via mixing phase compensated local oscillator
- Low pass filter to extract signal proportional to phase difference
- Apply gain



HDL Coder



Critical Path Report for hdl_all/QC_HDL

Summary Section

Critical Path Delay : 8.902 ns
Critical Path Begin : *HDL_BT_RM*
Critical Path End : *Unit Delay5*
Highlight Critical Path:
C:\Users\wubshet1\Documents\hdlcoder\92519_PRJ\hdlsrc\hdl_all\criticalPathEstimated.m
Highlight Uncharacterized blocks:
C:\Users\wubshet1\Documents\hdlcoder\92519_PRJ\hdlsrc\hdl_all\highlightCriticalPathEstimationOffen

Critical Path Details

Id	Propagation (ns)	Delay (ns)	Block Path
1	8.9020	8.9020	*HDL_BT_RM*
2	0.2980	-8.6040	*Unit Delay1*
3	8.8720	8.5740	*1-D Lookup Table*
4	8.9020	0.0300	*Unit Delay5*

- Generates customized VHDL to match Simulink functionality
- Pipelines to meet desired clock speed
- Modularizes VHDL libraries to mimic Simulink reference models
- Supports useful features in Simulink like data dictionaries
- Provides optimized blocks for certain operations

II vs USRP

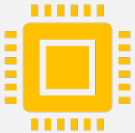
- 250MHz
- Depreciated drivers
- ISE generated bit file
- Interact with LabVIEW host with external C++ Library
- Interface requires modifications in VHDL

- 200MHz
- Modern platform
- Vivado generated bit file
- Interact with LabVIEW host with purely native LabVIEW code
- Interface requires minimal VHDL modifications, mostly defined and configured in LabVIEW

USRP Validation

Hello World

Moving Periodogram Testbench



Full QSCA Testing

Hello World

- Blinking LEDs
- Simple data processing and transfer
- Exploring how to interact with radio front end

NI LabVIEW for CompactRIO Developer's Guide

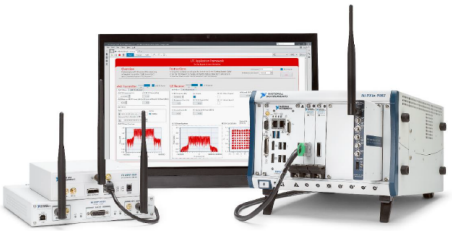
Recommended LabVIEW Architectures and Development Practices for Control and Monitoring Applications

SOFTWARE DEFINED RADIO HANDS ON:
FPGA PROTOTYPING WITH OVER-THE-AIR SIGNALS

Version 4.0

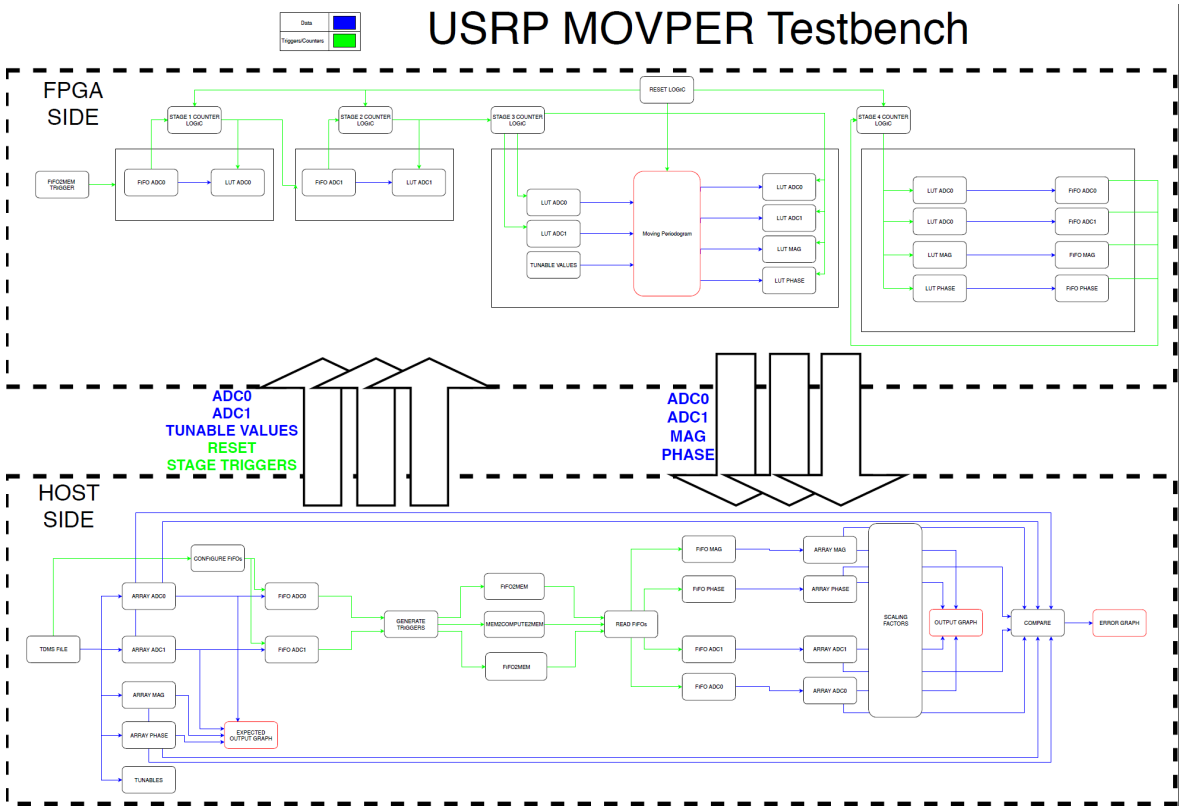
NI LabVIEW High-Performance FPGA Developer's Guide

Recommended Practices for Optimizing LabVIEW RIO Applications



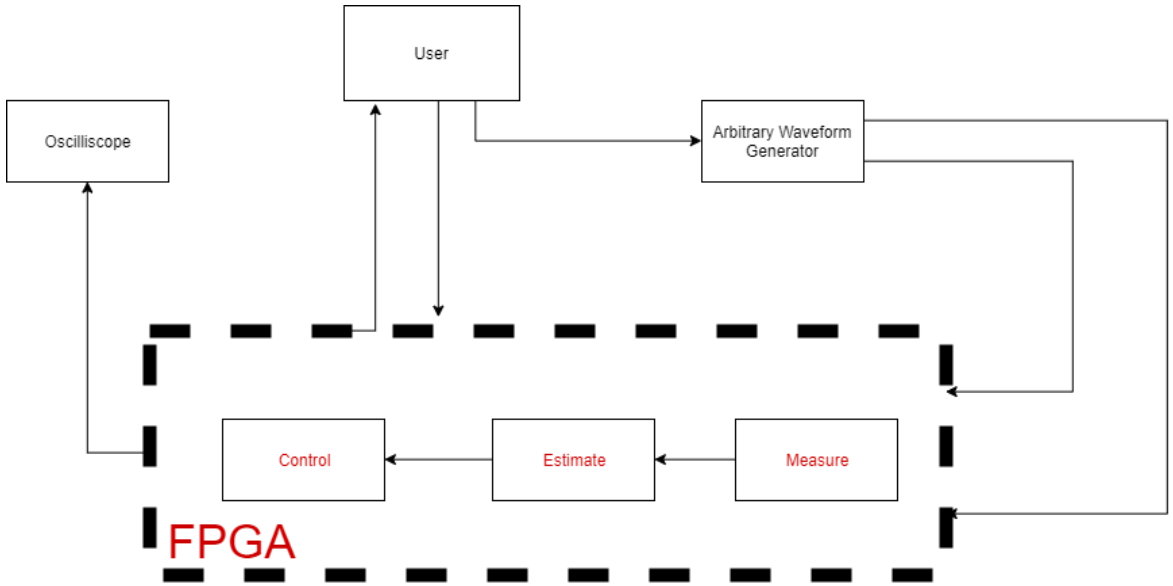
Moving Periodogram Testbench

- Using data collected and validated on the II as input to validate
  - Moving periodogram
  - Data transfer
- Using real AWG signals as stimulus

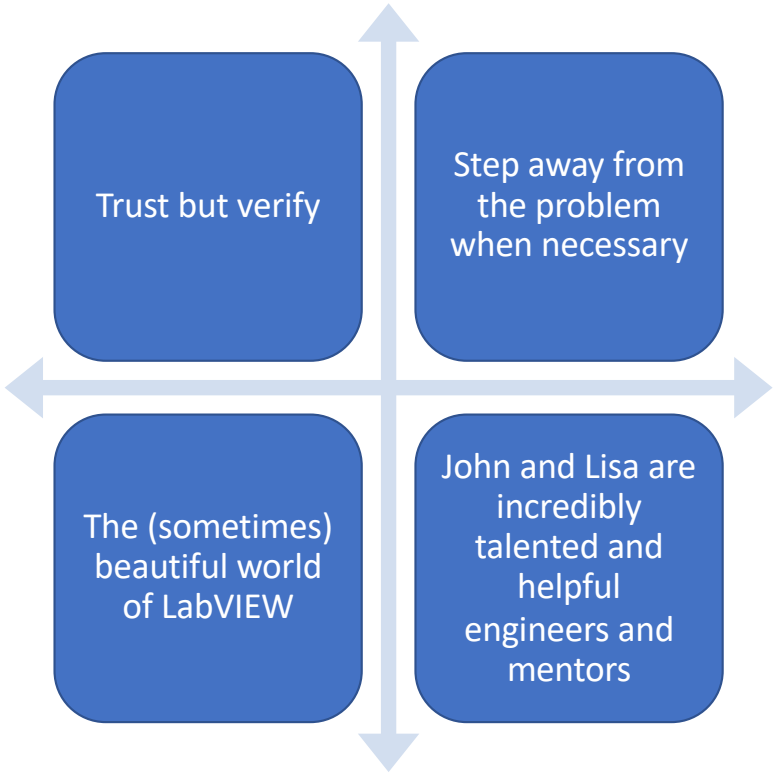


Full QSCA Testing

- Trigger source, AWG, scope, and USRP set up to mimic laboratory experimental apparatus
- Data processed and saved by updated LabVIEW host



What I've learned



Conclusion

The USRP *might* be a viable FPGA platform for quantum sensing and control and should be explored for quantum information research as well as axion detection research

Next Steps

COMPLETE DATA COLLECTION/ANALYSIS

COMPLETE THESIS

CODE REVIEW/HANDOFF

Future Work

- Closed loop control
- Full state feedback